POLISHING UNIFORMITY VIA PAD CONDITIONING

Field of the Invention

The present device relates generally to semiconductor devices and their fabrication and, more particularly, to chemical-mechanical polishing (CMP) tools for manufacturing and analyzing semiconductor devices.

Background of the invention

The electronics industry continues to rely upon advances in semiconductor manufacturing technology to realize higher-functioning devices while improving reliability and cost. For many applications, the manufacture of such devices is complex, and maintaining cost-effective manufacturing processes while concurrently maintaining or improving product quality is difficult to accomplish. As the requirements for device performance and cost become more demanding, realizing a successful manufacturing process becomes more difficult.

The increased complexity of semiconductor devices has lead to certain disadvantageous developments including uneven device surfaces, which become more prominent as additional levels are added to multilevel-interconnection schemes and circuit features are scaled to submicron dimensions. Typically, each level within the device is patterned, resulting in a surface with varied step-heights where metal forming the pattern remains on the surface.

Planarization is a term describing the surface geometry of a semiconductor device. Complete planarization occurs when the surface of the dielectric is flat, as in a plane. No planarization occurs when the surface of the dielectric directly models the surface of the metal pattern in the layer underneath. The degree of planarization refers to the degree to which the varied surface geometry can be planarized, or smoothed out into a planar surface. Varied surface geometry is often undesirable. Therefore, as additional layers are formed within devices, the required degree of planarization increases.

A commonly-used planarization process in semiconductor device manufacturing is chemical-mechanical polishing, or CMP. CMP is useful in the planarization of silicon wafers and of VLSI circuits between different manufacturing processes. CMP is a popular planarization method, due in part to its usefulness in the global planarization of semiconductor devices. Traditional planarization processes are restricted to effecting local planarity or topographical variation on a small scale, whereas CMP is often useful on a global scale greater than about ten microns, depending upon the CMP tool being used.

A CMP tool commonly includes a table for securing a wafer-polishing pad with a semiconductor wafer in a wafer holder arranged opposite the wafer-polishing pad. Typically, the wafer is located face-down on the polishing pad, and both the polishing pad and the wafer holder rotate. A slurry, typically including SiO_2 particles, is applied using a wand feeding to the wafer holder and pad. The rate of removal of material from the wafer is a combination of chemical and mechanical rates. The mechanical removal

rate is roughly proportional to the pressure and the relative velocity of the wafer. The chemical removal rate is a function of the size of the slurry particles and the slurry solution pH.

In addition to the use of slurry in the CMP process, a conditioner is typically used for conditioning the polishing pad. The conditioner aids in the CMP polishing process and contributes to the longevity of the pad.

A problem arises in connection with CMP processing when the rotating wafer carrier is in a position, relative to the rotating pad, that is considered center-offset. For example, the center-offset condition may include center-fast or center-slow conditions. The wafer carrier is in a position that is center-fast relative to the rotating pad when the center of the wafer is polished at a higher rate than the outer regions of the wafer. The wafer carrier is in a position that is center-slow relative to the rotating pad when the center of the wafer is polished at a lower rate than the outer regions of the wafer. The disparity in polishing rate of a wafer is attributable to non-uniform conditions. For example, the polish rate increases with increased pressure, increased slurry, or increased heat. When the wafer carrier is in a position relative to the rotating pad that results in higher pressure, higher heat, or increased slurry at the center of the wafer, the polish rate near the center increases relative to the polish rate near the edge.

In the past, these center-fast and center-slow conditions have been addressed by monitoring a set of wafers after each CMP run. For example, in connection with a CMP tool adapted to polish five wafers simultaneously, a run of five wafers would be polished and then inspected to determine whether they were experiencing a center-fast

or a center-slow state. Upon detecting a center-fast or a center-slow state, the oscillation amplitude was adjusted to compensate.

The consequences of center-fast or center-slow conditions can be severely disadvantageous. These conditions can result in damage to the pad and/or wafers processed using the pad; such damage includes, for example: long arc type scratches and shallow micro-scratches, die thickness variation, and the die containing residual slurry particles. Such damage can result in a wafer yield lost. Moreover, with the material and labor cost of each pad being in the hundreds of dollars, excessive occurrences of pad replacements can be a significant detriment.

Summary of the Invention

The present invention involves methods and arrangements directed to improving the CMP process, the improvements including but not limited to an expeditious CMP process, reduced maintenance to the CMP tool, enhanced pad wear, and increased wafer yield. The present invention is exemplified in a number of implementations and applications, some of which are summarized below.

According to an example embodiment, the present invention is directed to a method for chemical-mechanical polishing a wafer. A CMP arrangement having a polishing table and a wafer carrier adapted to carry a wafer relative to the center of the polishing table is used to polish the wafer. The pad is conditioned as a function of determining that the wafer is being polished in the center-offset manner. By using this method, the negative effects associated with center-offset polishing are diminished.

According to another example embodiment, the present invention includes a CMP polishing arrangement having a polishing pad, a wafer carrier, and a conditioning device. The wafer carrier is arranged to carry a wafer, rotate, and hold the wafer face-down on a polishing pad arranged to rotate and polish the wafer. A detection arrangement is adapted to detect whether the wafer is being polished in a center-offset manner. The conditioning device is arranged to condition the pad in response to the detection arrangement.

The above summary of the present invention is not necessarily intended to describe each illustrated embodiment or every implementation of the present invention. The figures and detailed description which follow more particularly exemplify these embodiments.

Brief Description of the Drawings

The invention may be more completely understood in consideration of the following detailed description in connection with the accompanying drawings, in which:

FIG. 1 shows a top view of an arrangement for a CMP process for polishing a semiconductor wafer, according to an example embodiment of the present invention;

FIG. 2 shows a cut-away side view of an arrangement for a CMP process for polishing a semiconductor wafer, according to another example embodiment of the present invention; and

FIG. 3 is a flow chart for a method for polishing a semiconductor wafer, according to another example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not necessarily to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description

The present invention is directed toward a new method for chemical-mechanical polishing (CMP) that improves the ability to obtain a uniform polish-rate of semiconductor wafers, longer life of the polishing pads used in the chemical-mechanical polishing process, faster throughput of semiconductor wafers, and reduced defects. According to an example embodiment of the present invention, a semiconductor wafer is arranged in a wafer carrier of a CMP apparatus having, in addition to the wafer carrier, a polishing table including a pad and a conditioning device, such as a conditioning wheel. The semiconductor wafer is polished and it is determined whether the polishing is proceeding in a center-offset manner such as center-fast or center-slow. For instance, one method for detecting whether the wafer is being polished in a center-offset manner is to remove the wafer from the carrier and measure the thickness across the wafer using a device such as a pair of calipers. The conditioning device is arranged over the pad and relative to the center of the polishing table as a function of whether the wafer is being polished in a center-offset manner and the pad is conditioned. In this manner, negative aspects of center-fast or center-slow polishing are addressed.

FIG. 1 shows a top view and FIG. 2 shows a side view of a CMP arrangement 100, according to another example embodiment of the present invention. The CMP arrangement includes a polishing table 210 having a polishing pad 140. The polishing table 210 is capable of rotation, such as shown by directional arrow 141. A wafer carrier 130 is arranged over the pad and adapted to carry a semiconductor wafer 135 and bring it in contact with the pad 140 for polishing. Although FIG. 1 shows the wafer

carrier 130 located directly over the pad 140, the wafer carrier 130 may be located with only a portion of the carrier 130 over the pad 140 in order to enhance the application of the present invention. The wafer carrier is further arranged to rotate, such as shown by directional arrow 131. Conditioning wheel 110 is arranged over the pad 140 and used to condition the pad, responsive to detecting center-offset polishing. Supply 120 is used to supply conditioning materials such as water or de-ionized water to the pad 140.

In another example implementation of the present invention, conditioning wheel 110 is further arranged relative to the center of the polishing table as a function of the detection of a center-fast condition, a center-slow condition, or the detection of neither a center-fast nor a center-slow condition. For example, although FIG. 1 shows the conditioning wheel arranged generally over the pad, the wheel may be arranged closer to the center, or closer to the edge of the pad 140. In addition, although shown by way of illustration in FIG. 1 as a wheel, the conditioning wheel 110 may include other types of pad conditioning devices.

FIG. 3 shows a flow diagram for a CMP method for addressing center-fast and center-slow polishing, according to another example embodiment of the present invention. The CMP method includes the use of a CMP apparatus having a table, a polishing pad, a wafer carrier and a conditioning device. A wafer is arranged in the wafer carrier at block 310, brought in contact with the pad and polished at block 320. If it is determined that the wafer is being polished in a center-fast manner at block 330, the conditioning device is arranged over the pad at block 340 and the pad is conditioned to correct center-fast polishing at block 350. If the wafer is not being polished in a center-

fast manner at block 330, it is determined whether the wafer is being polished in a center-slow manner at block 360. If the wafer is being polished in a center-slow manner, the conditioning device is arranged over the pad at block 370 and the pad is conditioned to correct center-slow polishing at block 380. If the wafer is not being polished in a center-slow manner, the polishing process is continued at block 390.

In a more particular example embodiment of the present invention, the conditioning device is arranged relative to the center of the polishing table in order to reduce the thickness of the polishing pad. When a particular portion of the polishing pad is thicker than the rest of the pad, that portion places greater pressure upon a wafer being polished, increasing the polish rate in that portion. By reducing the thickness, the polish rate is reduced at the thinned portion of the pad. Using this embodiment in connection with the discovery of a center-fast or a center-slow polishing condition, the pad can be thinned in the region of the pad that is polishing faster. In doing so, the pressure on the wafer from that region is reduced, and the polish rate decreases due to the reduction in pressure.

For example, FIG. 2 shows a pad that has been thinned near the edge. The thickness A at the center of the pad is greater than the thickness B near the edge of the pad. When a wafer is held against the pad having the edge thinned, the center of the wafer can be held at a location of the pad having greater thickness than the edge. Due to the greater thickness near the center, the wafer is polished center-fast. Alternatively, the center of the pad could be thinned resulting in the edge having a greater thickness

relative to the center thickness prior to thinning and enhancing center-slow polishing. In another alternative, various portions of the pad could be thinned.

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes may be made thereto. For example, many features of the above embodiments are combinable in a single conditioner arrangement and/or conditioning process. Such changes do not depart from the spirit and scope of the present invention, which is set forth in the following claims.